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Notice of Allowability

Application No.

10/021,133

Examiner

Matthew A. Henry

Applicant(s)

WANG ET AL.

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to ____.
2. ☒ The allowed claim(s) is/are 1 - 17.
3. ☐ The drawings filed on ____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
(b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date ____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other ____. |

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Drawings

2. The drawings filed on 10/29/2001 are acceptable subject to correction of the informalities indicated below.

In Figure 3, Item 126 is supposed to be connected to both Item 304 and 306. According to the specification, Items 304 and 306 both share a direct connection to Item 126. In the drawings, it is clear that Item 306 is directly connected to Item 126. Item 304 does not clearly share this same direct connection. By drawing the connection line from Item 126 to 304 directly through Item 306, it calls into question whether Item 306 affects the input to Item 304.

In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Title

3. The title has been changed to: Method for synchronizing multiple serial data streams using a plurality of clock signals.

4. The following is an examiner's statement of reasons for allowance:

5. In regards to Claim 1, Leighou discloses:

A system for synchronizing a plurality of data channels (Column 2, Lines 8-12),
the system comprising:

“a core circuit having a clock distribution circuit, the core circuit providing a plurality of data streams at a frequency of a core clock signal carried by the clock distribution circuit,” (Columns 3 and 4, Lines 67-68 and 1-3, respectively).

“a first phase-locked loop circuit generating a plurality of clock signals,”
(Column 9, Lines 3-5).

“a plurality of channel circuits,” (Column 2, Lines 19-20).

Leighou fails to disclose:

“a first clock signal from the plurality of clock signals [that] has the same frequency and substantially the same phase as the core clock signal carried by the clock distribution circuit.”

“channel circuits coupled to the core circuit and to the first phase-locked loop circuit, the channel circuits converting the plurality of data streams, received at a frequency of the first clock signal, into a plurality of serial data streams at a frequency of a second clock signal from the plurality of clock signals.”

The prior art fails to disclose or suggest a motivation for the employment of a plurality of a clock signals with well-defined frequency relationships with each other all of which are generated from a single PLL and are utilized in serial data transmission. Therefore, it would not have been obvious to a person of ordinary skill in the art at the time of invention to modify Leighou to incorporate the features described above.

6. In regards to Claim 10, Leighou discloses:

A method of synchronizing a plurality of data channels (Column 2, Lines 8-12),
the method comprising:

“receiving a reference clock signal,” (Column 11, Lines 16-20).

“generating a plurality of clock signals based on the reference clock
signal,” (Column 9, Lines 3-5).

“receiving the data, transferred through the plurality of data paths, by
corresponding channel circuits at a clock rate,” (Column 5, Lines 52-54).

“transforming the data received by each of the channel circuits from a
parallel to a serial data stream at a clock rate,” (Column 4, Line 11).

Leighou fails to disclose:

“providing a core clock signal from the plurality of clock signals to a core
circuit, wherein data is transferred from the core circuit through a plurality of data
paths at a clock rate of the core clock signal,”

“receiving the data, transferred through the plurality of data paths, by
corresponding channel circuits at a clock rate of a first clock signal from the
plurality of clock signals, the first clock signal having the same frequency and
substantially the same phase as the core clock signal,”

“transforming the data received by each of the channel circuits from a
parallel to a serial data stream at a clock rate of a second clock signal from the
plurality of clock signals.”

The prior art fails to disclose or suggest a motivation for the employment of a
plurality of a clock signals with well-defined frequency relationships with all of which are

generated from a single source and are utilized in serial data transmission. Therefore, it would not have been obvious to a person of ordinary skill in the art at the time of invention to modify Leighou to incorporate the features described above.

7. In regards to Claim 16, Leighou discloses:

“A first phase-locked loop circuit generating a plurality of clock signals, including a first clock signal,” (Column 9, Lines 3-5).

Leighou fails to disclose:

“a plurality of channel circuits, coupled to the first phase-locked loop circuit, that each receive a data stream from a core circuit at a frequency of a core clock signal which has the same frequency and substantially the same phase as the first clock signal, wherein at least one of the plurality of clock signals is distributed to at least some of the plurality of channel circuits via a register-to-register transfer.”

The prior art fails to disclose or suggest a motivation for the employment of a plurality of a clock signals with well-defined frequency relationships with each other all of which are generated from a single PLL and are utilized in serial data transmission. This is further true for the transmission of some of the signals generated by the PLL from channel circuit to channel circuit. Therefore, it would not have been obvious to a person of ordinary skill in the art at the time of invention to modify Leighou to incorporate the features described above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Herbert teaches of the use of multiple clock frequencies being generated from a single PLL, however it fails to discuss the use of these frequencies over a plurality of data channels.

Rapport implements multiple input frequencies to a plurality of channels, however these multiple inputs do not actually have a different frequency. In this case, the multiple inputs relate to time delay.

Doblar connects a plurality of data channels to a PLL, However, the outputs of the PLL is not a plurality, nor is there a core circuit pushing data into the data channels.

The prior art listed above is considered to be relevant to the state of the art and demonstrative of the patentability of the above application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600 2100

MAH